

# HD14021B

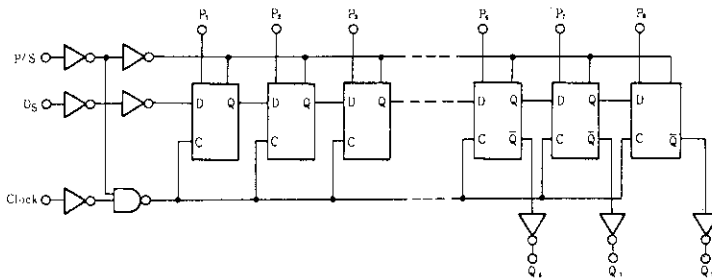
## 8-bit Static Shift Register

The HD14021B 8-bit Static shift register finds primary use in parallel-to serial data conversion, asynchronous parallel input, serial output data queuing; and other general purpose register applications requiring low power and/or high noise immunity.

### FEATURES

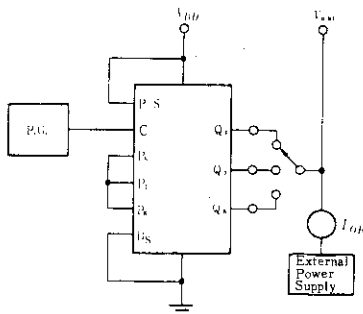
- Quiescent Current = 5nA/pkg typ. @5V
- Asynchronous Parallel Input/Serial Output
- Full Static Operation from DC to 7MHz
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

### LOGIC DIAGRAM

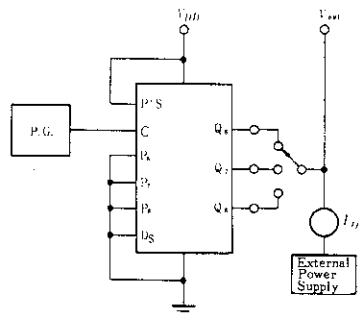


### DC CHARACTERISTIC TEST CIRCUIT

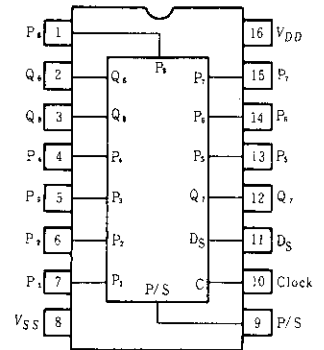
•  $I_{OH}$



•  $I_{OL}$



### PIN ARRANGEMENT



(Top View)

### TRUTH TABLE

#### Serial Operation

t	Clock	D <sub>n</sub>	P/S
n	↗	0	0
n+1	↗	1	0
n+2	↗	0	0
n+3	↗	1	0
	↘	x	0

Q <sub>6</sub>	Q <sub>7</sub>	Q <sub>8</sub>
t = n+6	t = n+7	t = n+8
0	?	?
1	0	?
0	1	0
1	0	1
Q <sub>6</sub>	Q <sub>7</sub>	Q <sub>8</sub>

#### Parallel Operation

Clock	D <sub>n</sub>	P/S	D <sub>m</sub>	Q <sub>m</sub> *
↗	x	1	0	0
↗	x	1	1	1

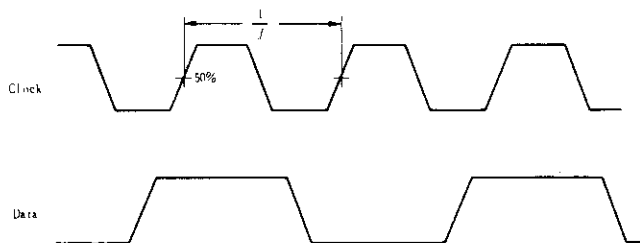
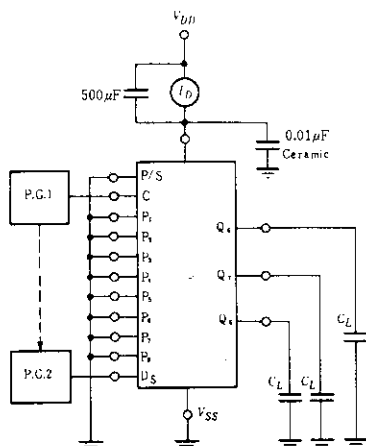
注) \* : Q<sub>6</sub>, Q<sub>7</sub>, & Q<sub>8</sub> are available externally  
 x : Don't Care

**■ ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	$V_{OL}$	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	$V_{OH}$	5.0	$V_{in}=0$ or $V_{DD}$	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	$V_{IL}$	5.0	$V_{out}=4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	$V_{out}=0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	$I_{OH}$	5.0	$V_{OH}=2.5V$	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	$V_{OH}=4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	$V_{OH}=9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—	
	$I_{OL}$	5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—	
Input Current	$I_{in}$	15		—	$\pm 0.3$	—	$\pm 0.00001$	$\pm 0.3$	—	$\pm 1.0$	$\mu A$
Input Capacitance	$C_{in}$		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	$I_{DD}$	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	$\mu A$
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	$I_T$	5.0	Dynamic + $I_{DD}$ , per Gate	—	—	—	0.76	—	—	—	$\mu A$
		10	per Gate	—	—	—	1.51	—	—	—	
		15	$C_L=50pF, f=1kHz$	—	—	—	2.27	—	—	—	

\* To calculate total supply current at frequency other than 1kHz.  
 @  $V_{DD}=5.0V$   $I_T=(10.75\mu A/kHz)f+I_{DD}$ . @  $V_{DD}=10V$   $I_T=(1.50\mu A/kHz)f+I_{DD}$ . @  $V_{DD}=15V$   $I_T=(2.25\mu A/kHz)f+I_{DD}$

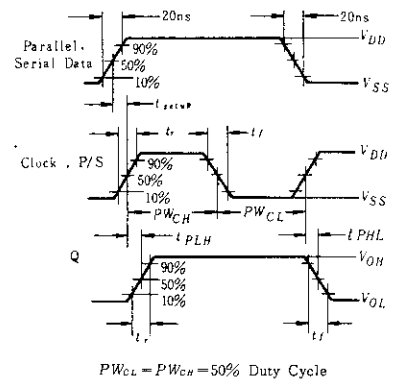
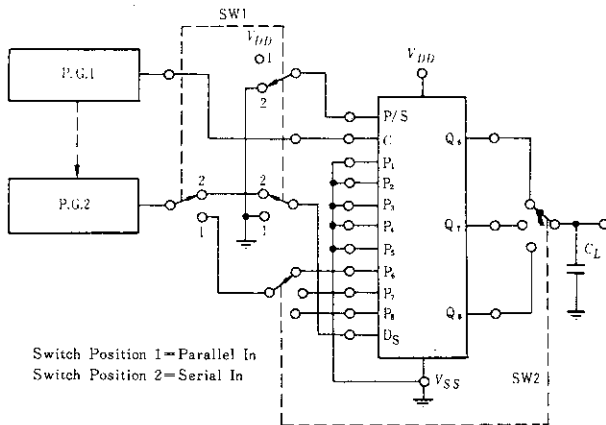
**■ POWER DISSIPATION TEST CIRCUIT AND WAVEFORM**



■ SWITCHING CHARACTERISTICS ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ (V)	min	typ	max	Unit
Output Rise Time	$t_r$	5.0	—	180	400	ns
		10	—	90	200	
		15	—	65	160	
Output Fall Time	$t_f$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	37	80	
Propagation Delay Time	$t_{PLH}$	5.0	—	400	1000	ns
		10	—	170	400	
	$t_{PHL}$	15	—	115	265	
Clock Pulse Width	$PW_C$	5.0	500	150	—	ns
		10	200	75	—	
		15	150	40	—	
Clock Frequency	$f_c$	5.0	—	3.0	1.0	MHz
		10	—	6.0	2.5	
		15	—	8.0	3.0	
Parallel/Serial Control Pulse Width	PW (P/S)	5.0	500	150	—	ns
		10	200	75	—	
		15	150	40	—	
Setup Time	$t_{setup}$	5.0	500	150	—	ns
		10	100	50	—	
		15	80	30	—	
Input Clock Rise Time	$t_{rc}$	5.0	—	—	15	ns
		10	—	—	15	
		15	—	—	15	

■ SWITCHING TIME TEST CIRCUIT





Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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